

FIG. 1

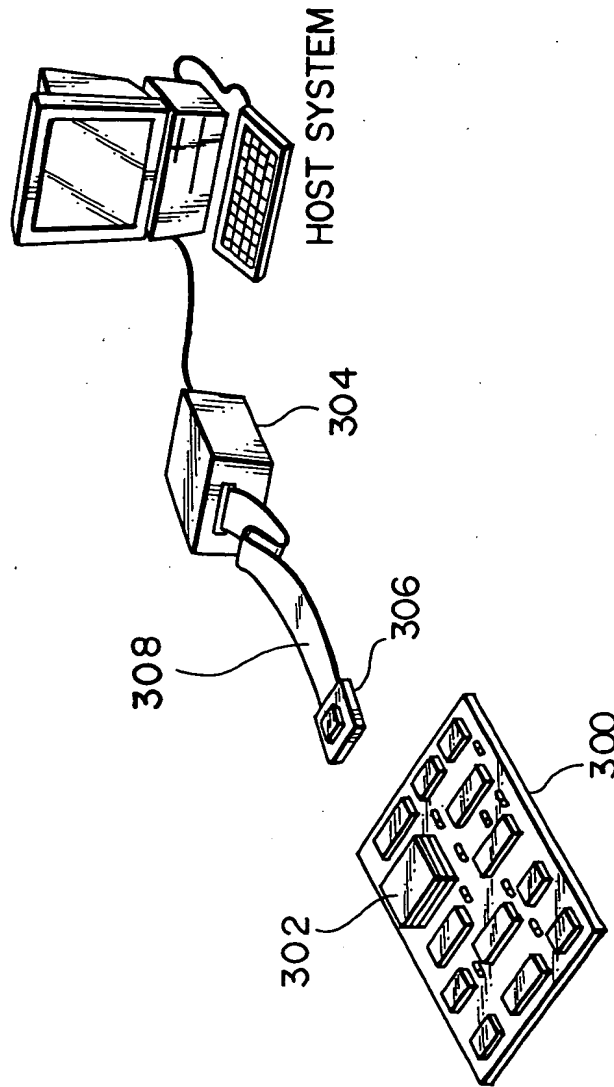


FIG. 2A

USER MODE

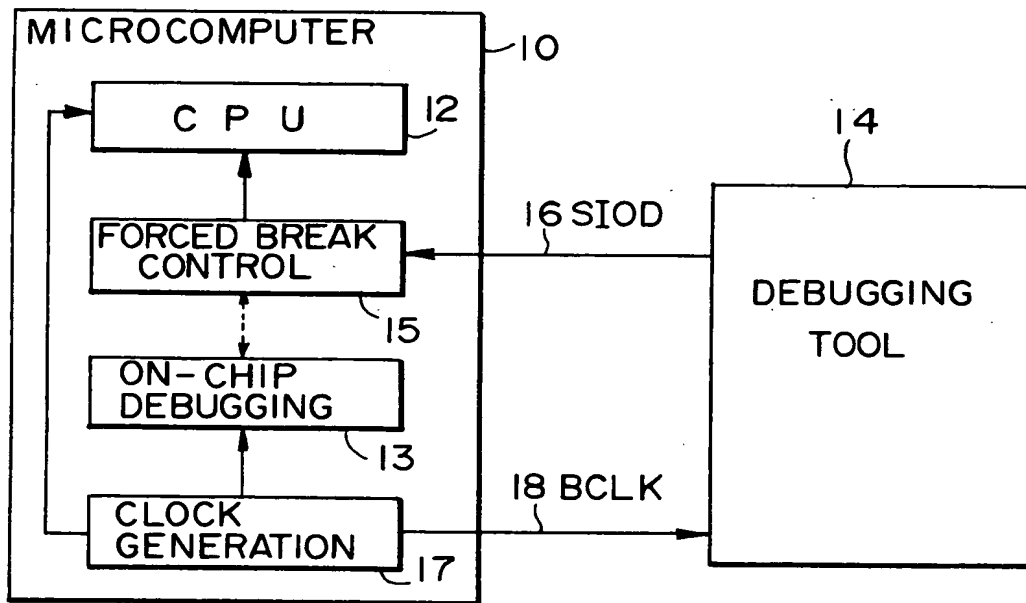
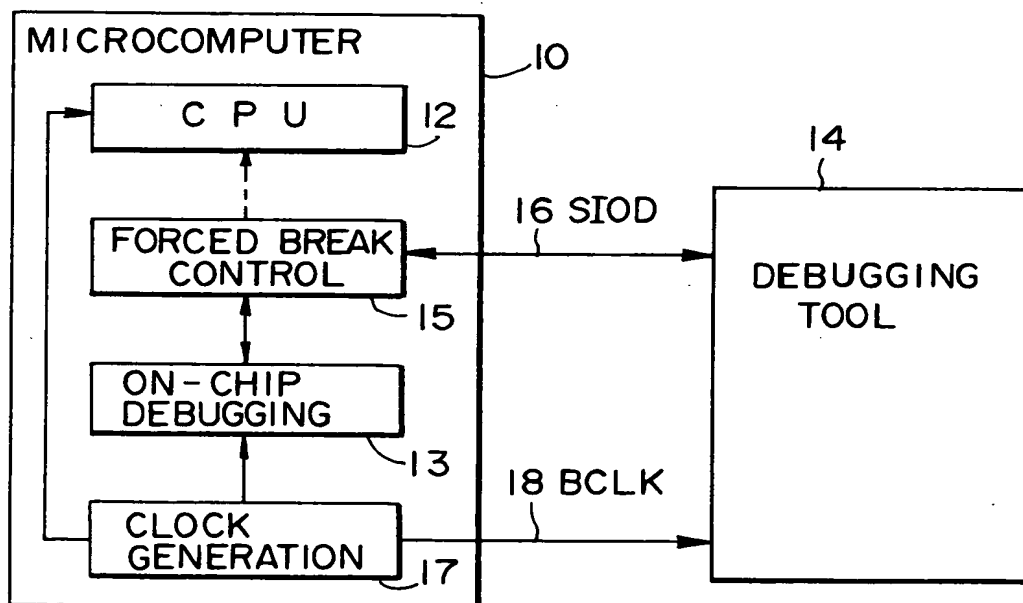


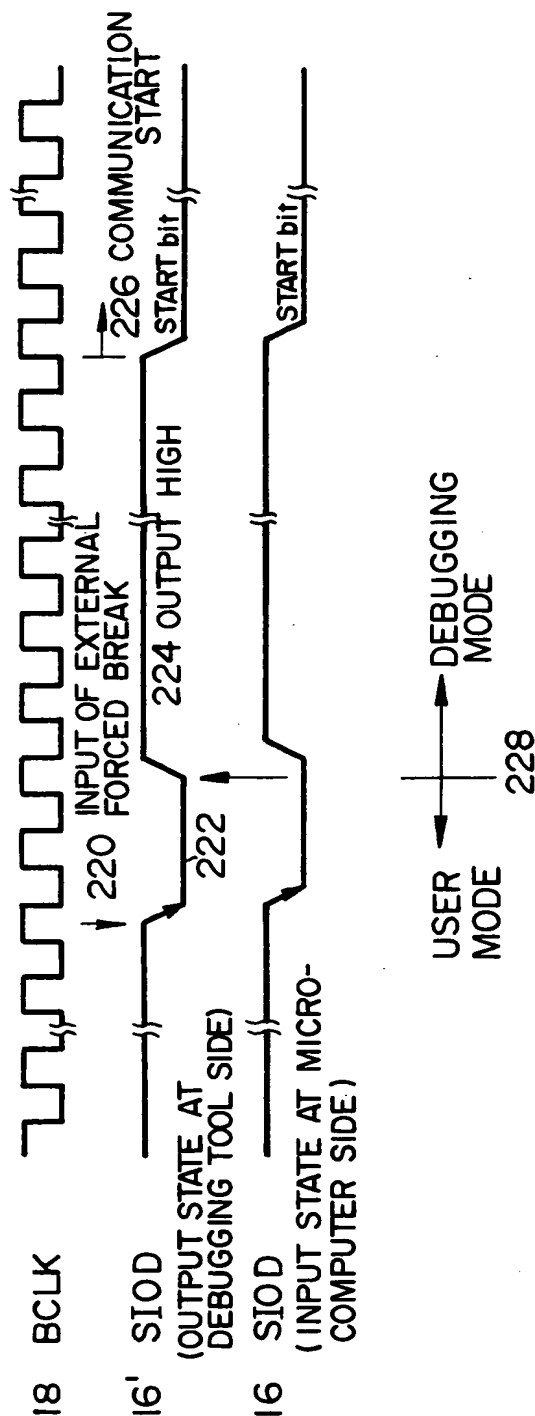
FIG. 2B

DEBUGGING MODE



3 / 17

FIG. 3



4/17

FIG. 4A

WHEN NO DEBUGGING TOOL IS CONNECTED

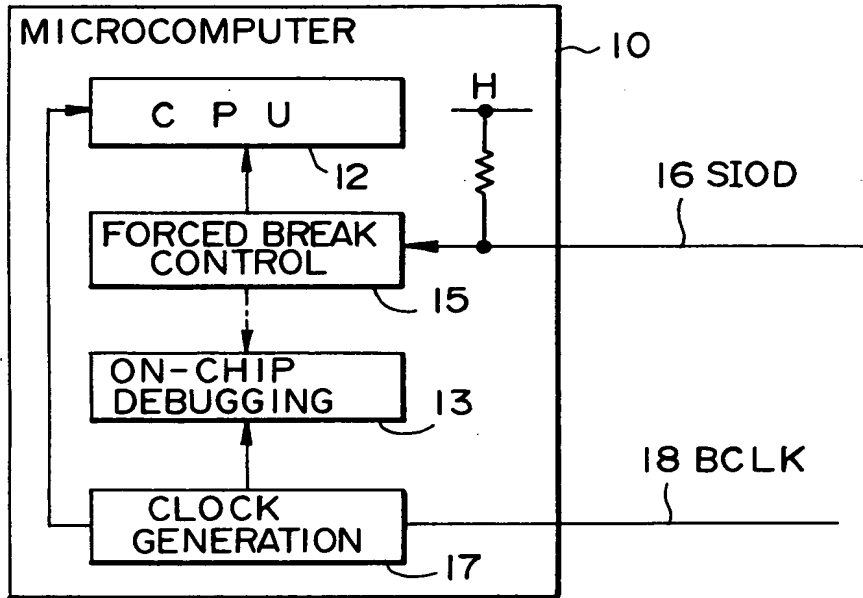


FIG. 4B

WHEN DEBUGGING TOOL IS CONNECTED

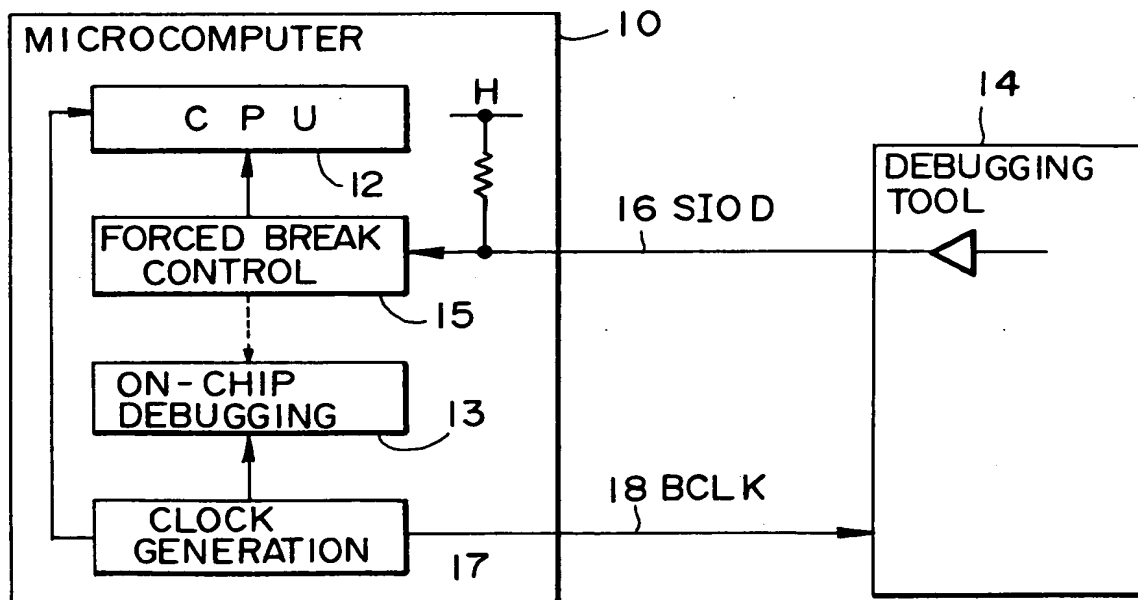


FIG. 5A

WHEN NO DEBUGGING TOOL IS CONNECTED

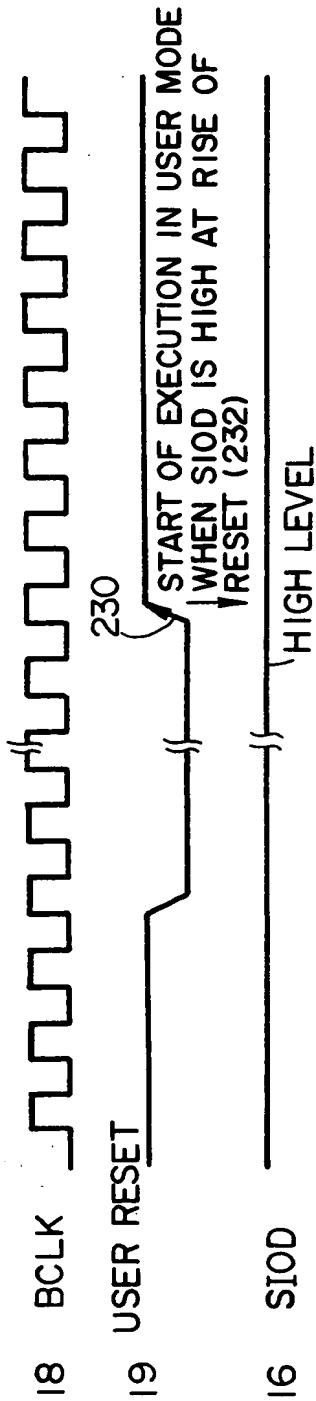
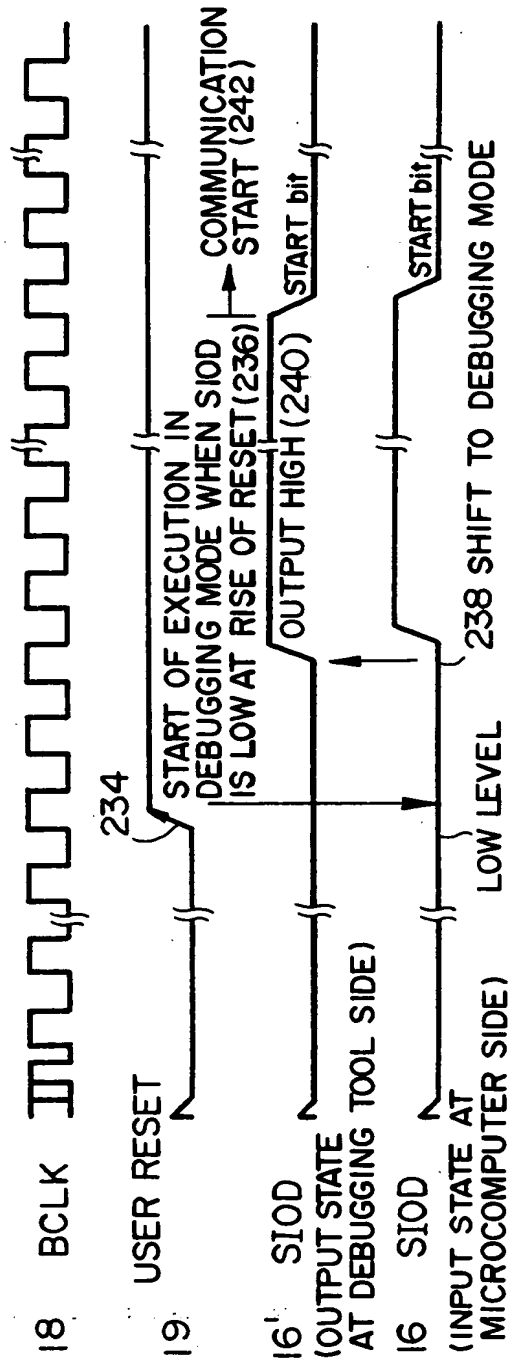


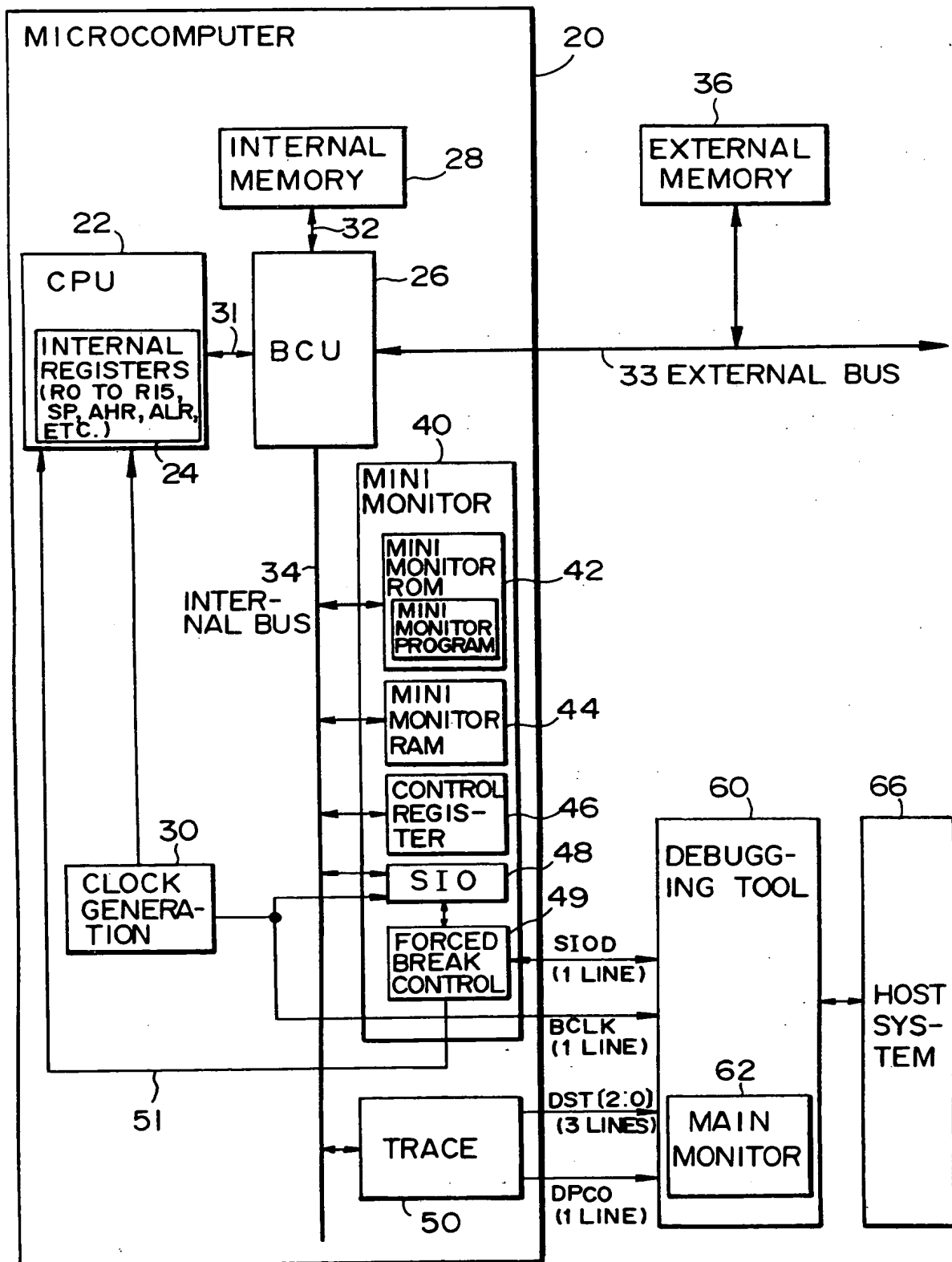
FIG. 5B

WHEN DEBUGGING TOOL IS CONNECTED



7/17

FIG. 7



8 / 17

FIG. 8

MEMORY MAP IN DEBUGGING MODE

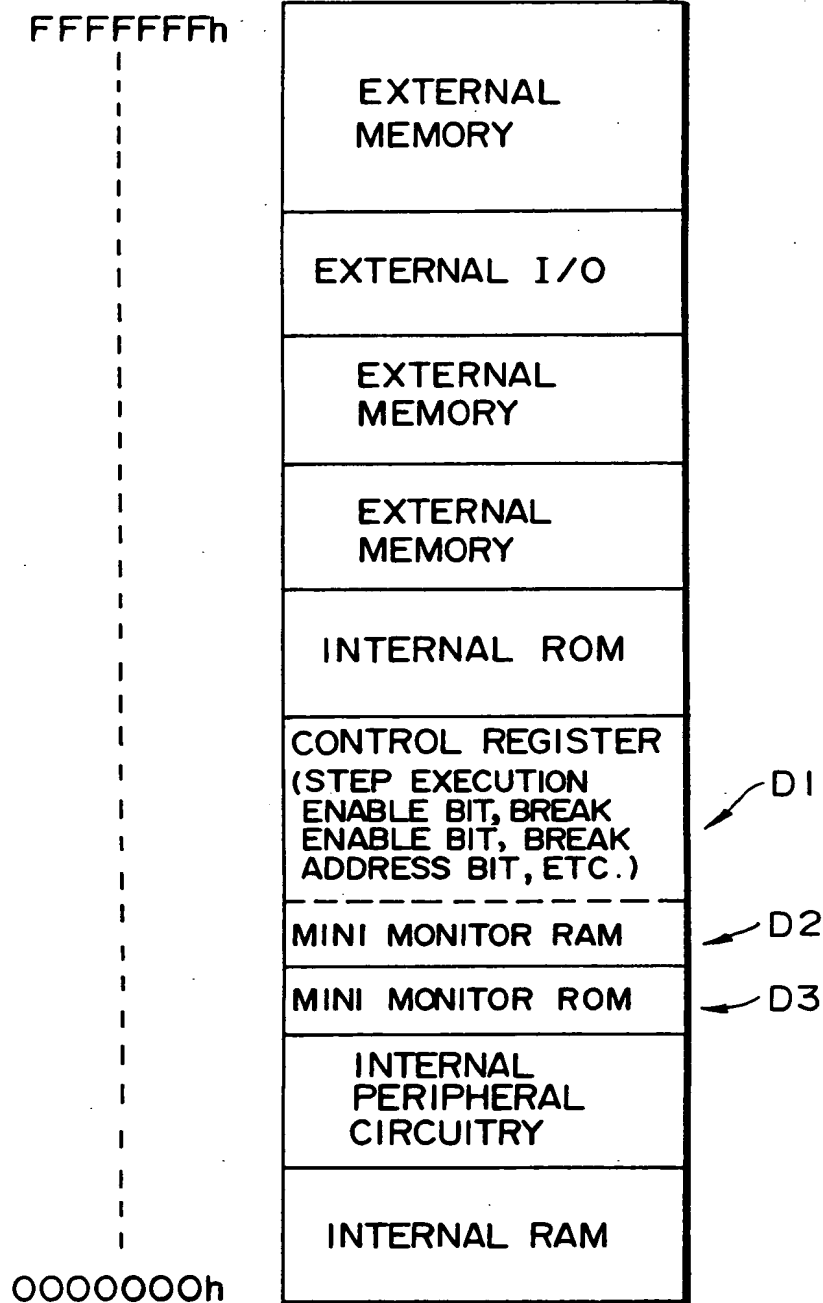


FIG. 9A

PROGRAM LOAD

$\left(\begin{array}{l} 80010h, 12 \text{ BYTES, ADD} \text{---, SUB} \text{---} \\ \text{AND} \text{---, OR} \text{---, XOR} \text{---, LD.W} \text{---} \end{array} \right) \Rightarrow \begin{array}{l} \text{WRITE}(80010h, \text{ADD} \text{---, SUB} \text{---}) \\ + \text{WRITE}(80014h, \text{ADD} \text{---, OR} \text{---}) \\ + \text{WRITE}(80018h, \text{XOR} \text{---, LD.W} \text{---}) \end{array}$

FIG. 9B

STEP EXECUTION \Rightarrow WRITE TO STEP EXECUTION ENABLE
 BIT OF CONTROL REGISTER
 +GO

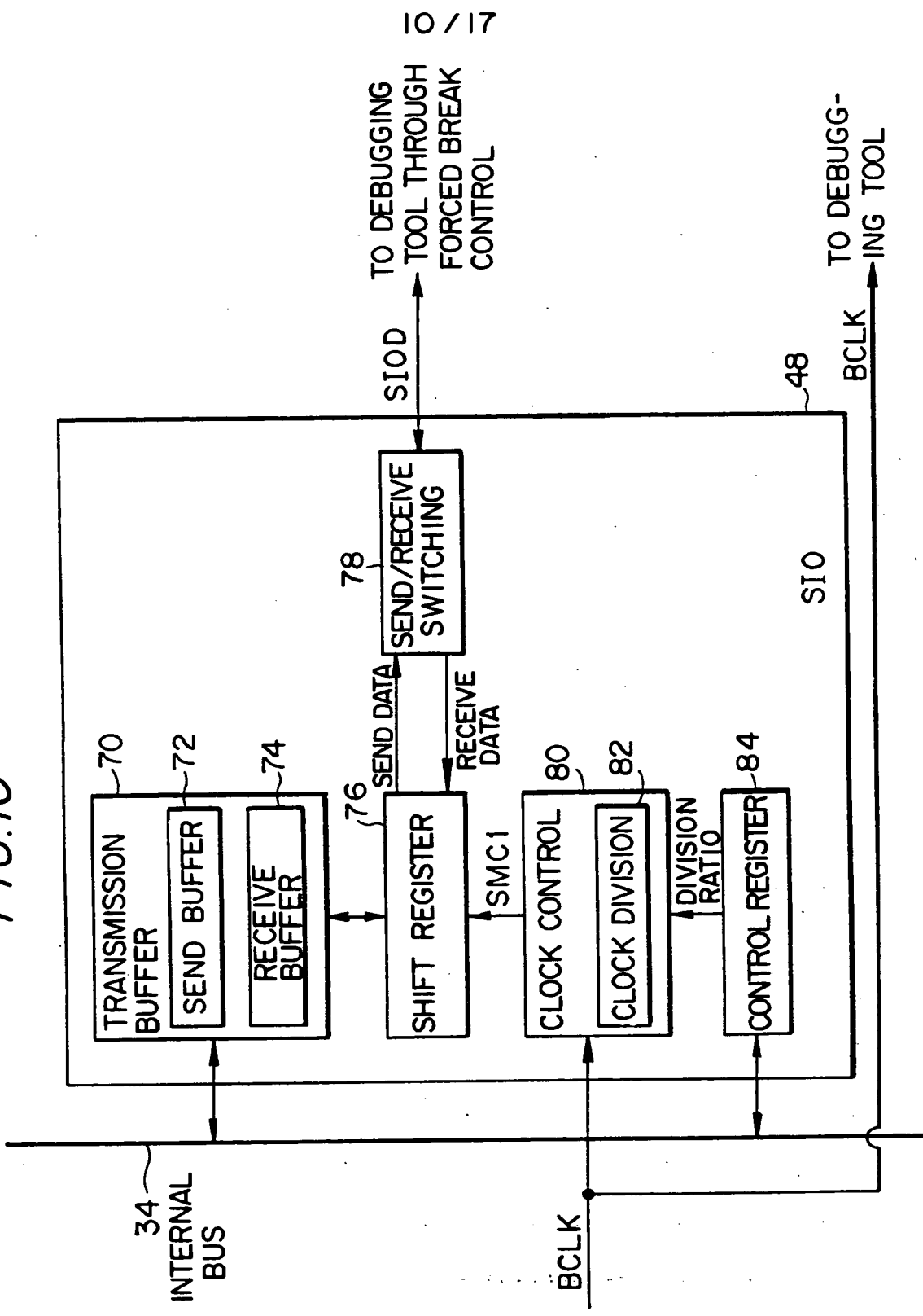
FIG. 9C

INTERNAL REGISTER READ \Rightarrow READ OF MONITOR RAM ON MEMORY MAP

FIG. 9D

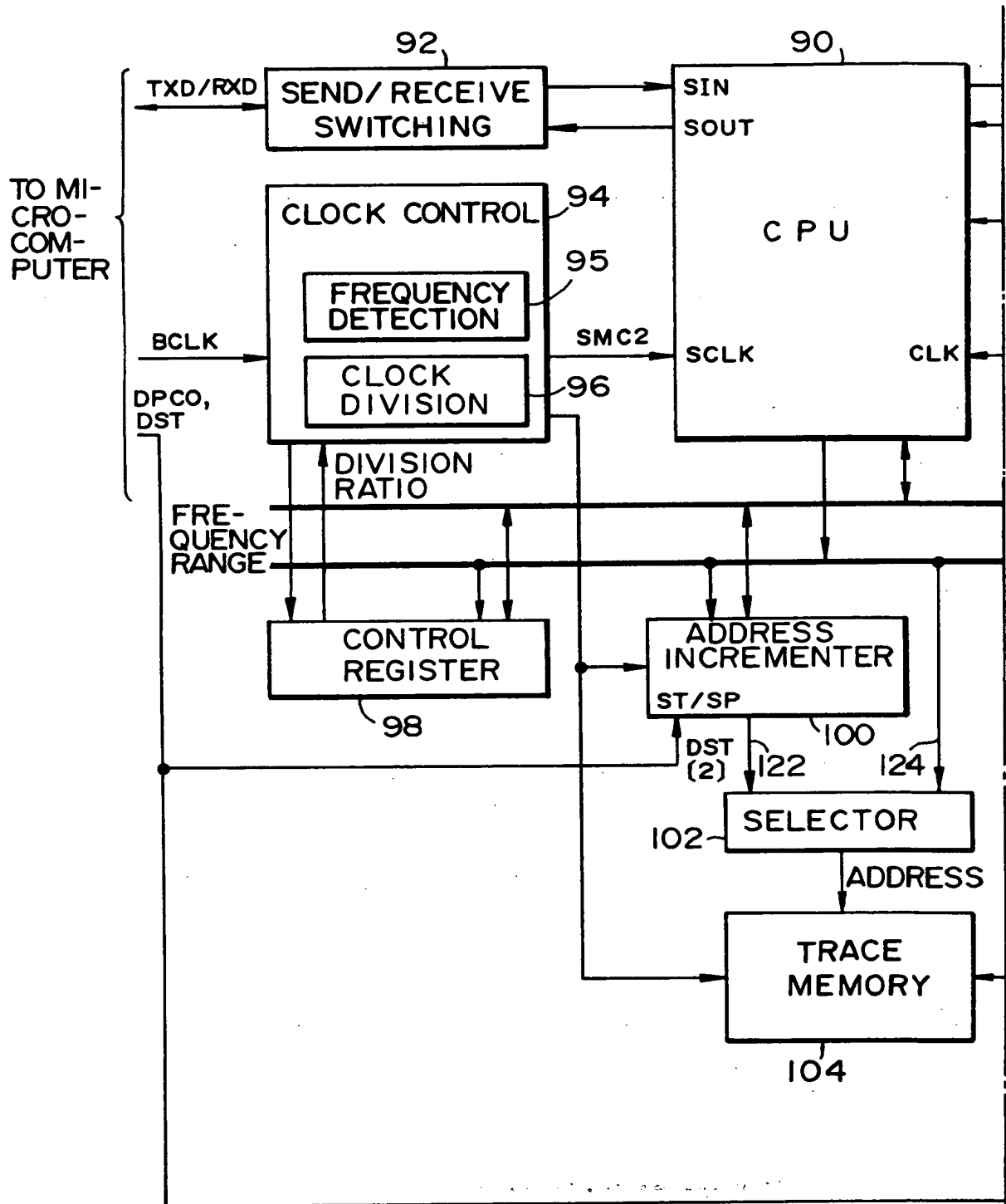
BREAKPOINT SETTING \Rightarrow WRITE TO BREAK ENABLE BIT AND
 BREAK ADDRESS BIT OF CONTROL
 REGISTER

FIG. 10



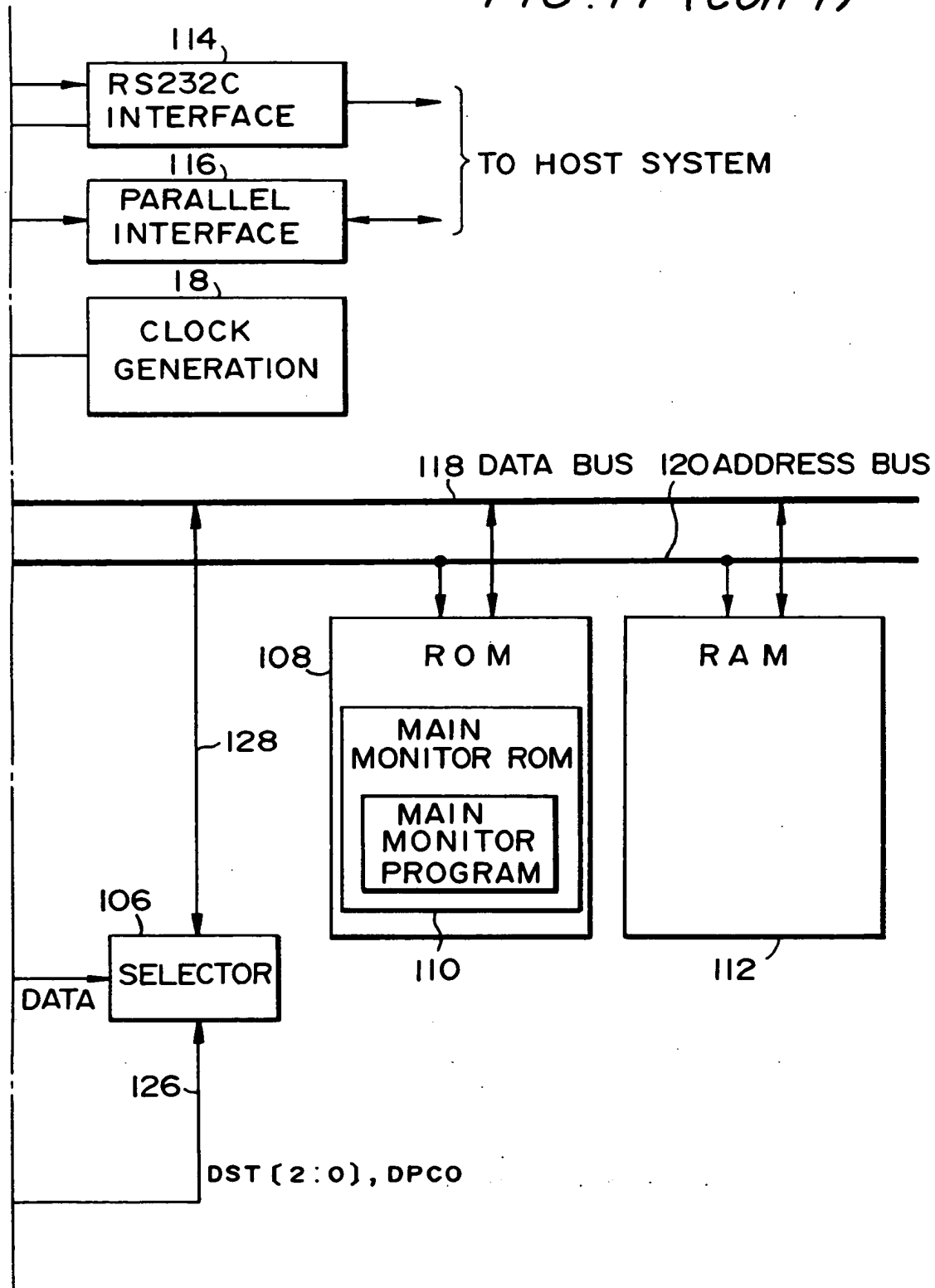
11/17

FIG. 11



11/17 (con't)

FIG. 11 (con't)



12 / 17

FIG. 12A

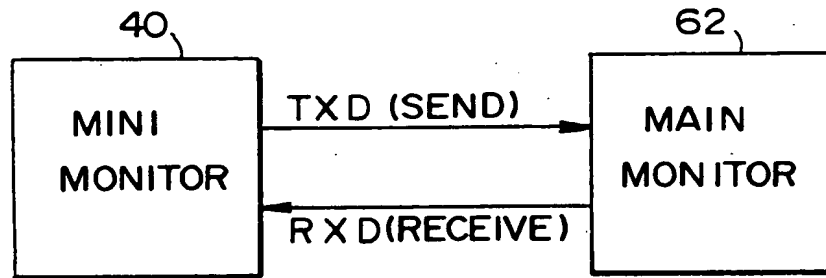


FIG. 12B

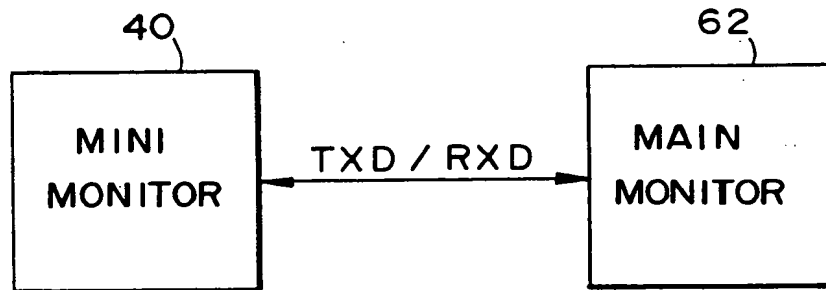
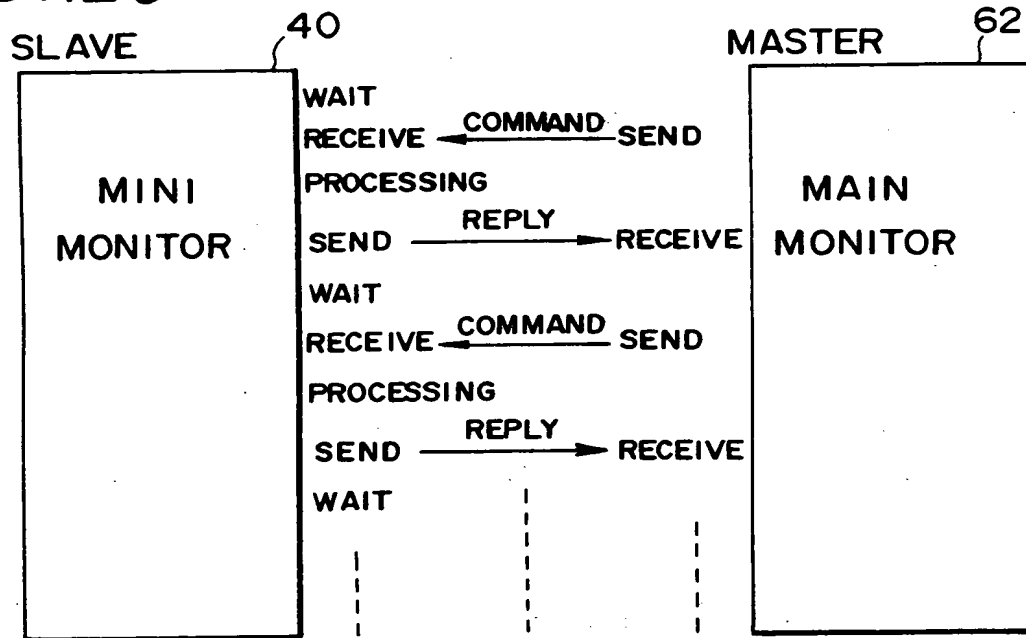
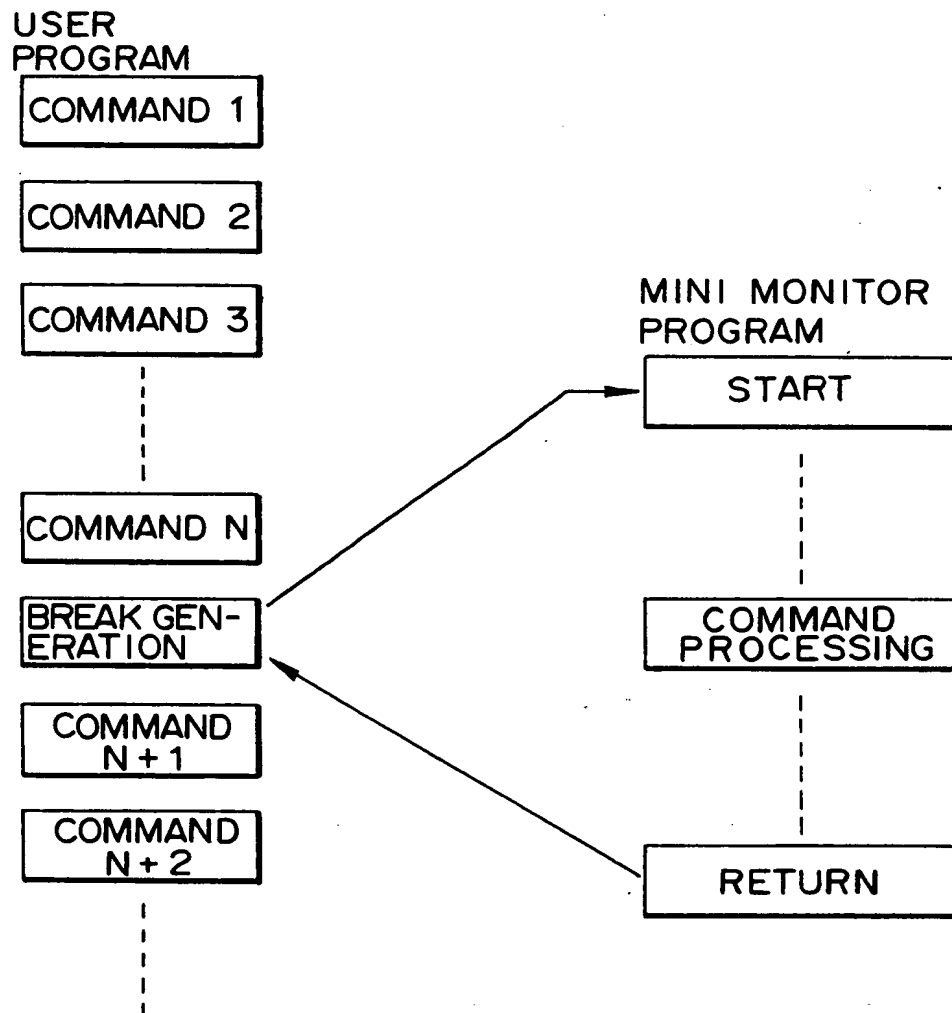


FIG. 12C



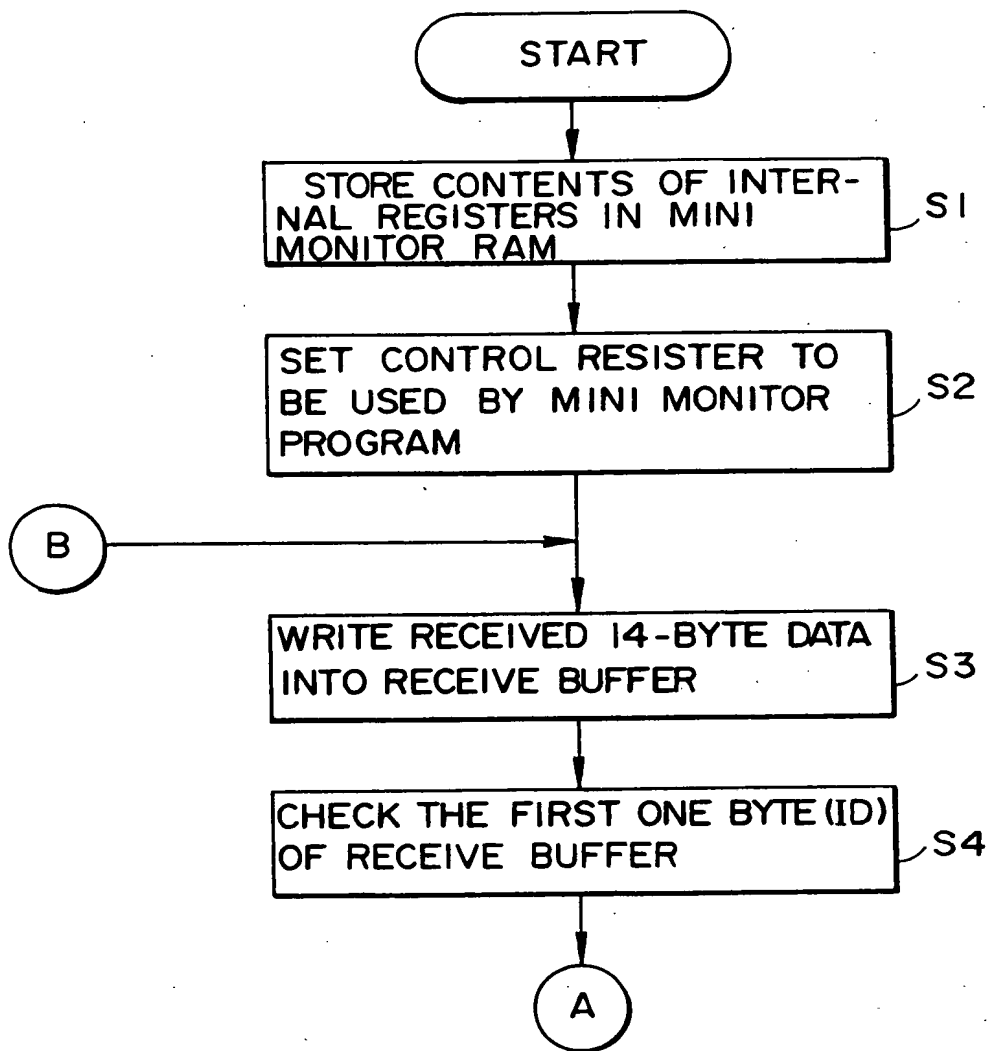
13 /17

FIG. 13



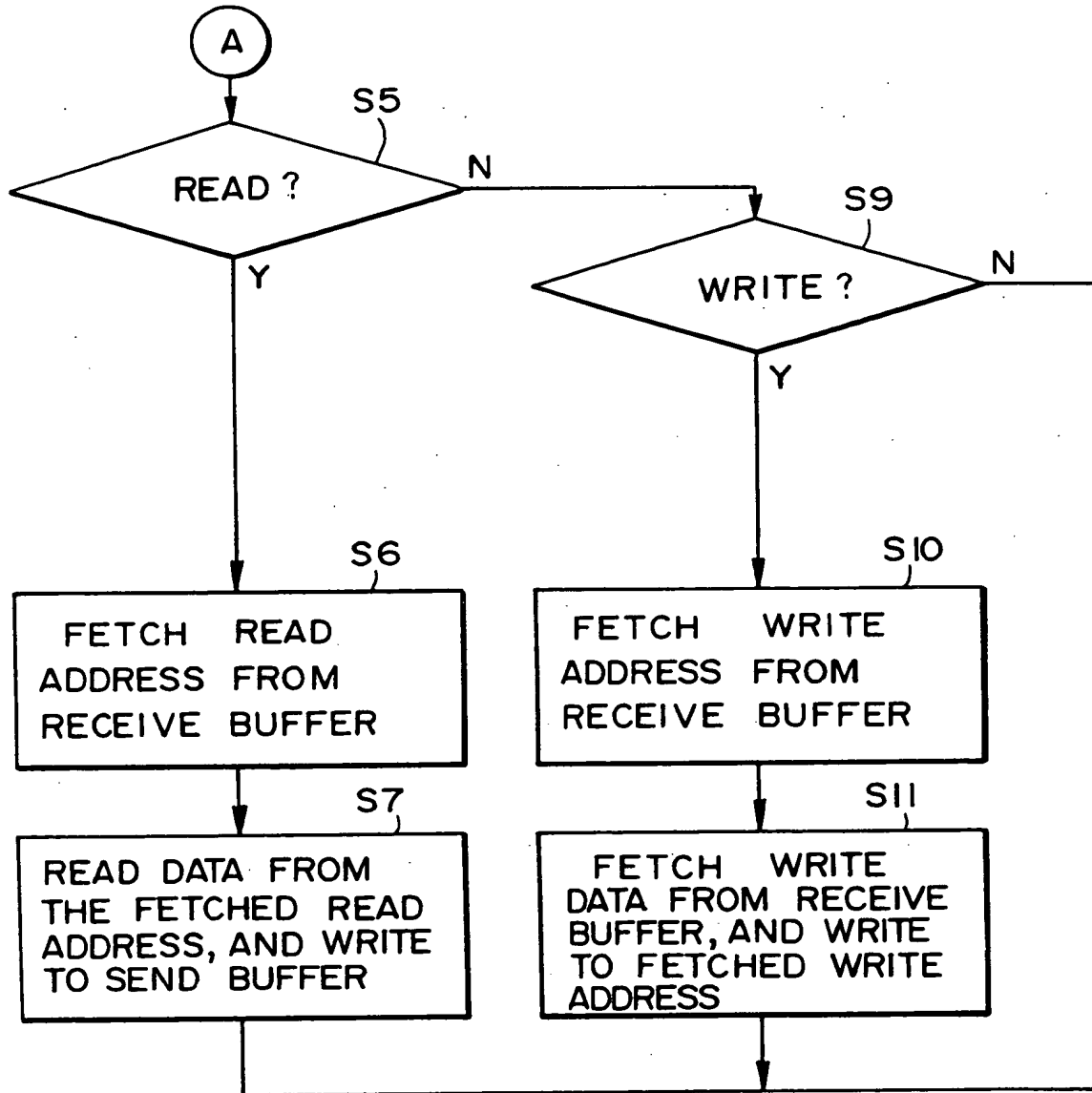
14/17

FIG. 14



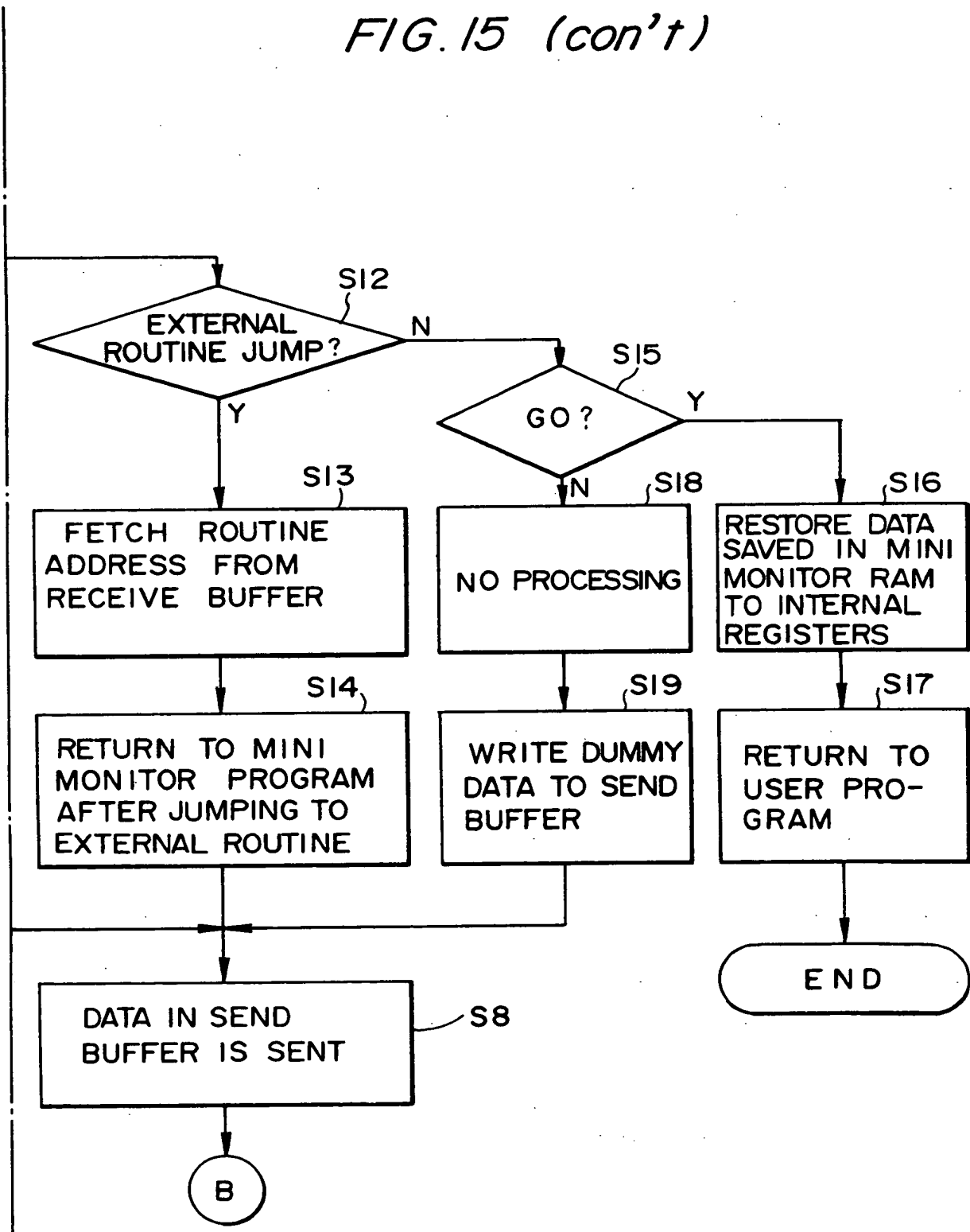
15 / 17

FIG. 15



15 / 17 (con't)

FIG. 15 (con't)



16/17

FIG. 16A

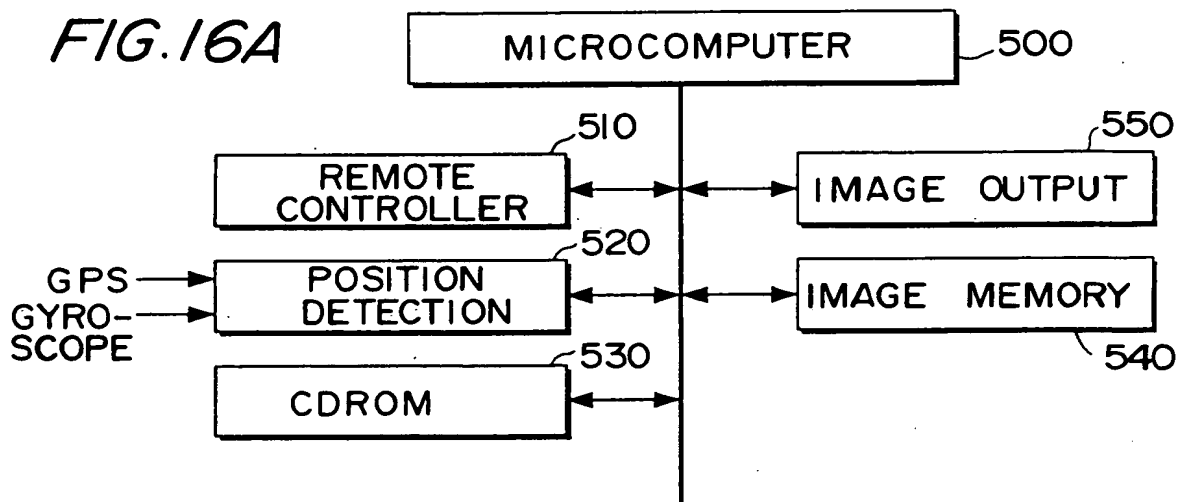


FIG. 16B

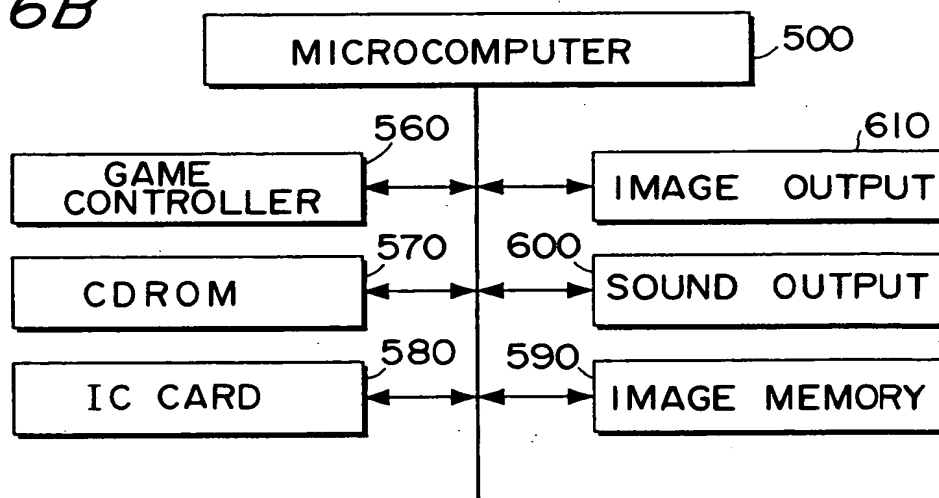
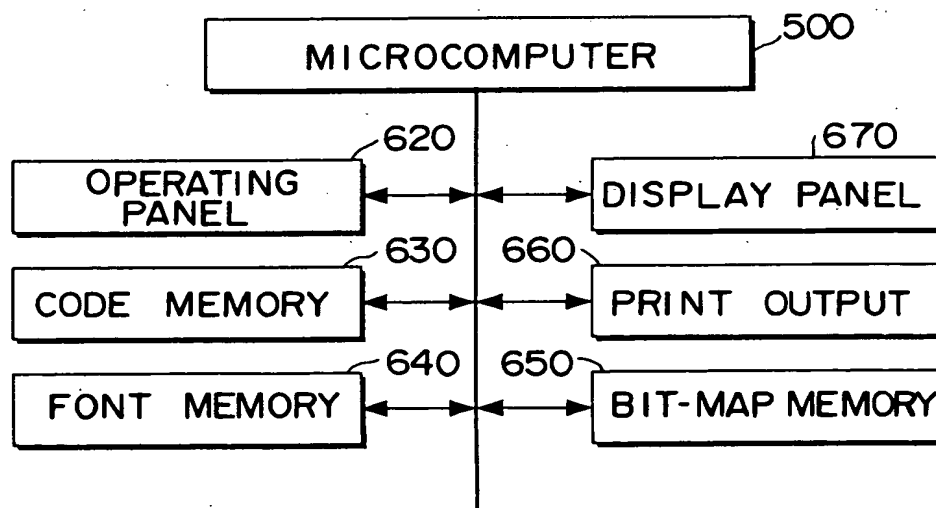


FIG. 16C



17/17

FIG.17A

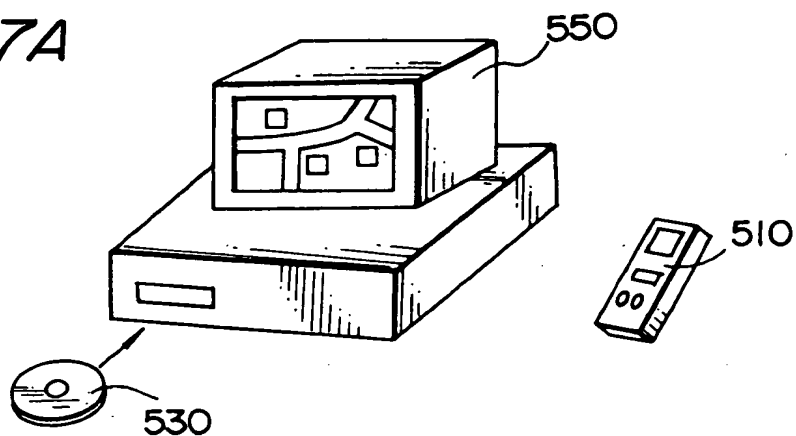


FIG.17B

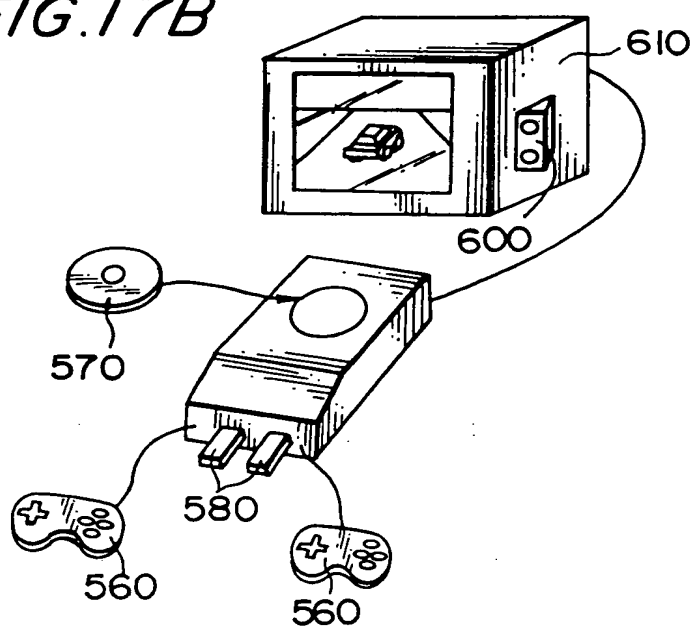


FIG.17C

